IDEC Chip Design Contest

A 90.8%-Efficiency SIMO Resonant Regulating Rectifier Generating 3 Outputs in a Half Cycle with Distributed Multi-Phase Control for Wirelessly-Powered Implantable Devices

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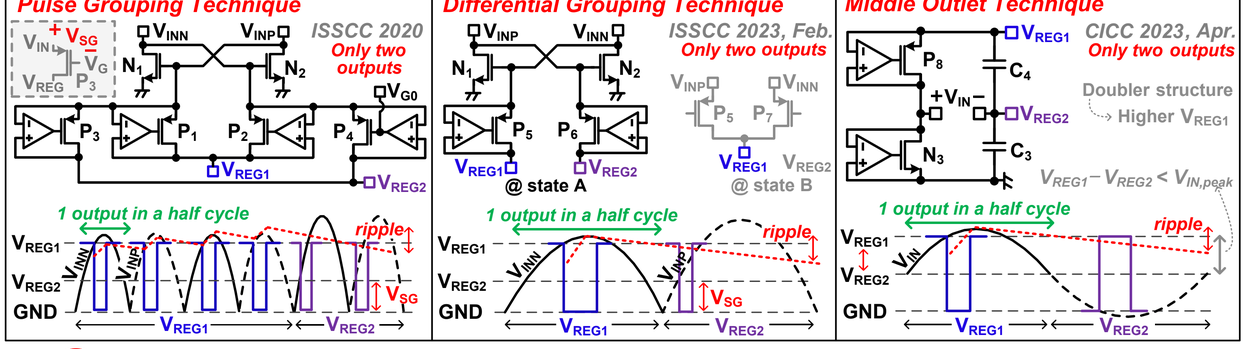
Motivation

Problem of Conv. Dual-Output R^3

Conventional Dual-Output Resonant Regulating Rectifier (R^3)

Dual-Output PWFM R^3 [1]	Dual-Output Synchronized PFM R^3 [2]	Dual-Output Voltage Doubler R^3 [3]
Pulse Grouping Technique	*Differential Grouping Technique*	*Middle Outlet Technique*
ISSCC 2020 Only two outputs	ISSCC 2023, Feb. Only two outputs	CICC 2023, Apr. Only two outputs



☹ **FIVE Challenges** in the **conventional dual-output R^3**

Challenge-1 : Low V_{SG} (V_{INN}-V_{G0}) in P_3 → High R_{ON} (on-resistance) & Entry in sub-thre mode

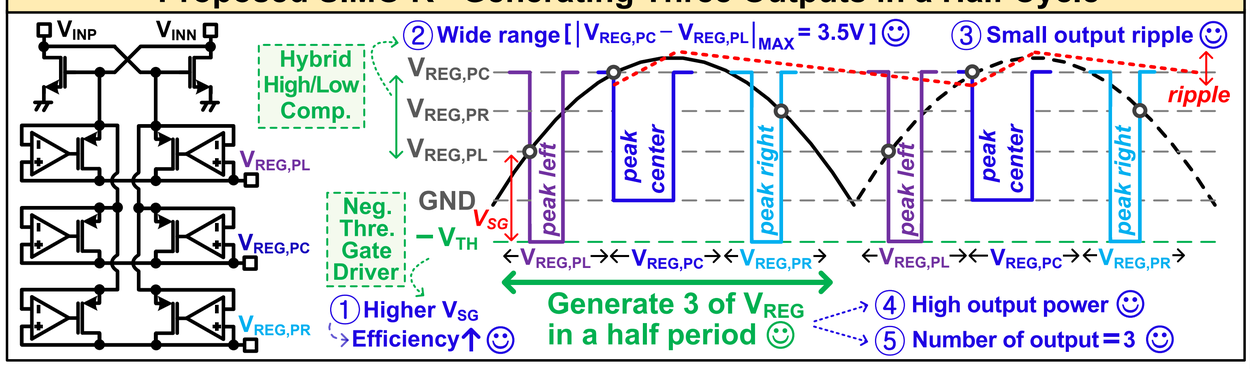
Challenge-2 : Narrow output range of V_{REG2} → $V_{REG2,MAX}-V_{REG2,MIN}\downarrow$ & $|V_{REG1}-V_{REG2}|_{MAX}\downarrow$

Challenge-3 : High output ripple → Unstable supplies

Challenge-4 : Low output power → Unapplicable for high-power system

Challenge-5 : Low number of outputs → Low efficient in dynamic voltage scaling stimulation

Proposed SIMO R^3 Generating Three Outputs in a Half Cycle



☺ **Negative threshold gate driver** solve ← Challenge-1

☺ **Hybrid high/low comparator** solve ← Challenge-2

☺ **Distributed multi-phase control in a half cycle** solve ← Challenge-3, 4, 5

Efficiency up to 90.8%
V_{REG2}: 1V - 3.5V 3 outputs

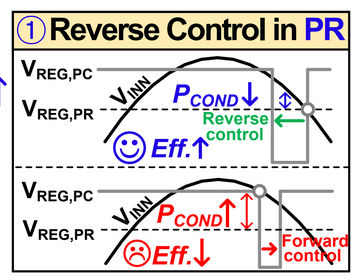
Detailed Circuits

New Circuit Techniques

4 Techniques in PR Total Comparator

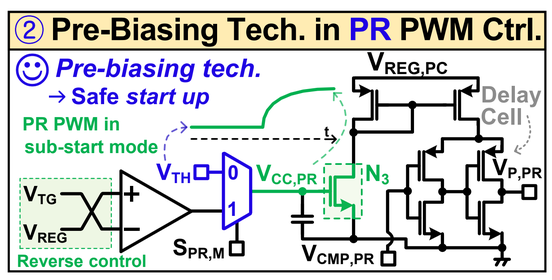
① *Reverse Control* → Eff↑
② *Pre-Biasing Tech.* → *Safe start up*
③ *Neg. Th. Gate Driver* → Eff↑ at low V_{REG}
④ *Hybrid H/L CMP & SEL.* → $|V_{REG,PC}-V_{REG,PL}|_{MAX}$↑

① Reverse Control in PR



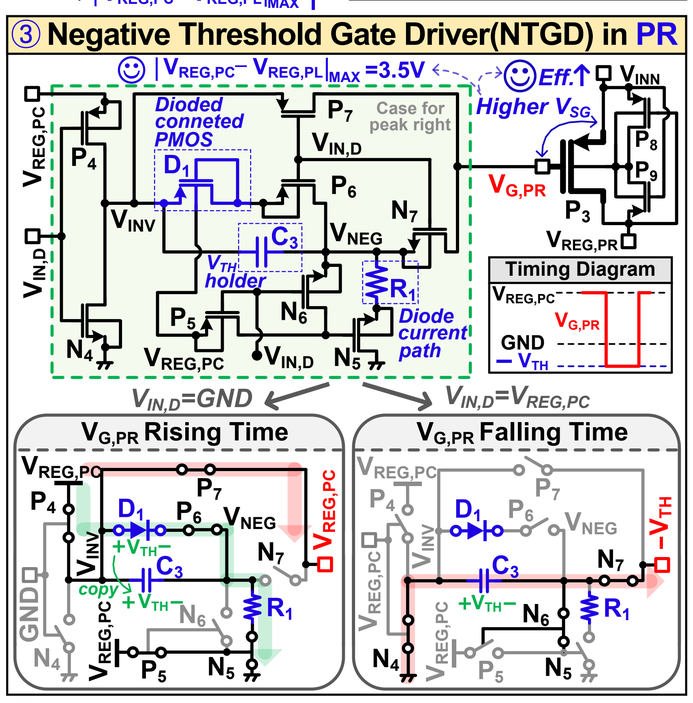
② Pre-Biasing Tech. in PR PWM Ctrl.

☺ *Pre-biasing tech.* → *Safe start up*



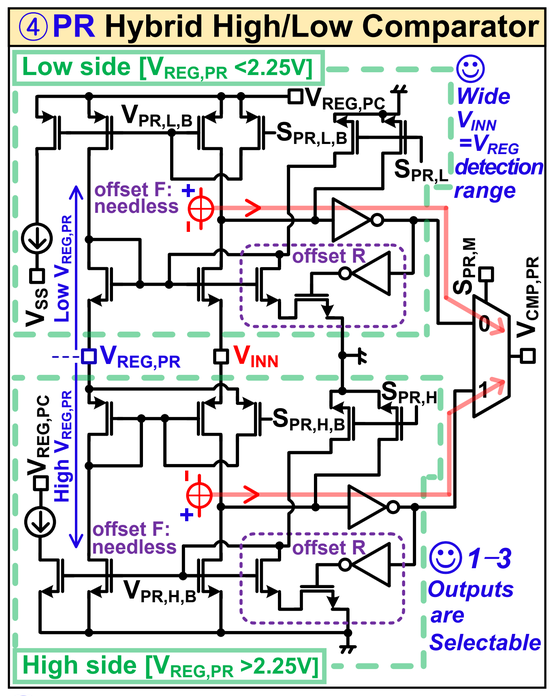
③ Negative Threshold Gate Driver(NTGD) in PR

☺ $|V_{REG,PC}-V_{REG,PL}|_{MAX}$ =3.5V ☺ Eff.↑ Higher V_{SG}



④ PR Hybrid High/Low Comparator

Low side [$V_{REG,PR}$ <2.25V] ☺ Wide V_{INN} =V_{REG} detection range



☺ **Reverse control technique**
→ High efficiency in PR region

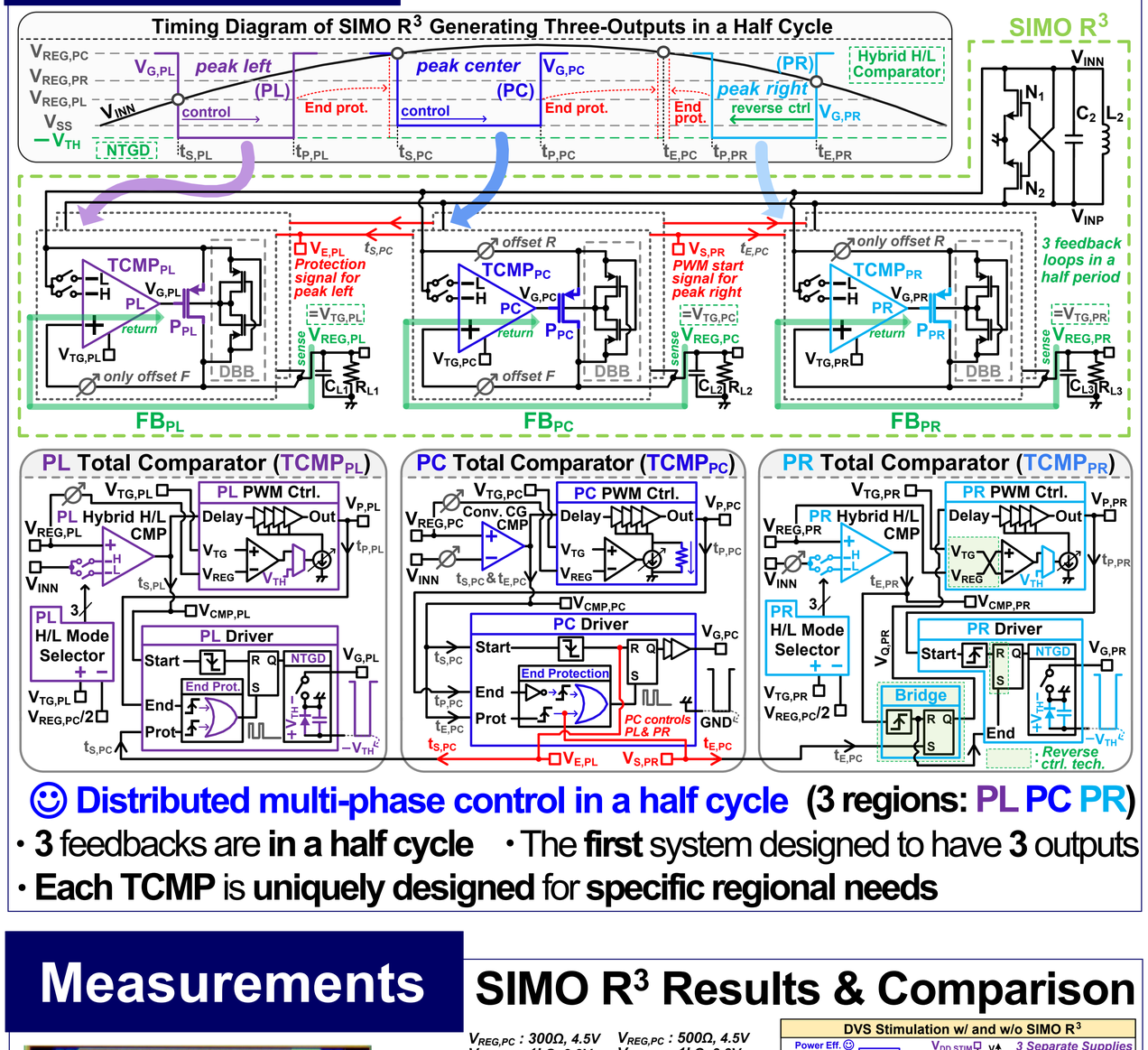
☺ **Pre-biasing technique**
→ Safe start-up in PR & PL region

☺ **Negative threshold gate driver**
→ High efficiency at low V_{REG} in PR & PL region

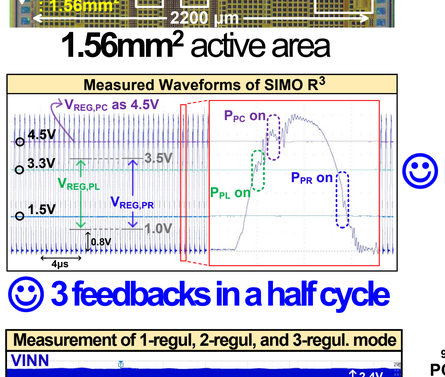
☺ **Hybrid high/low comparator**
→ High V_{REG} range in PR & PL region

Architecture

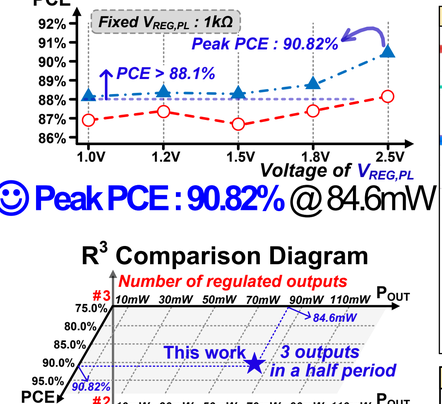
The Proposed R^3 : SIMO R^3



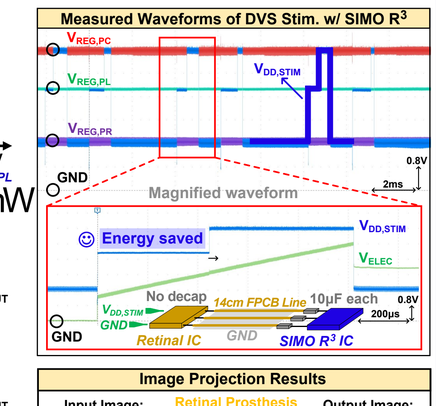
PL Total Comparator ($TCMP_{PL}$)



PC Total Comparator ($TCMP_{PC}$)



PR Total Comparator ($TCMP_{PR}$)

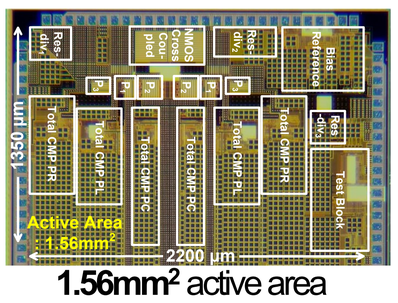


☺ **Distributed multi-phase control in a half cycle** (3 regions: PL PC PR)

- **3** feedbacks are **in a half cycle**
- The **first** system designed to have **3** outputs
- **Each TCMP** is **uniquely designed** for **specific regional needs**

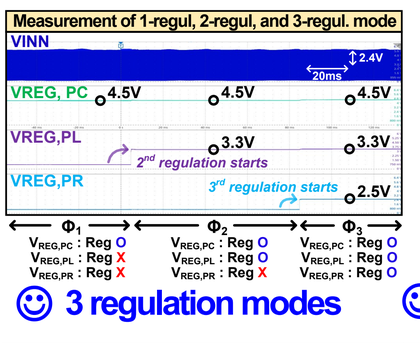
Measurements

SIMO R^3 Results & Comparison

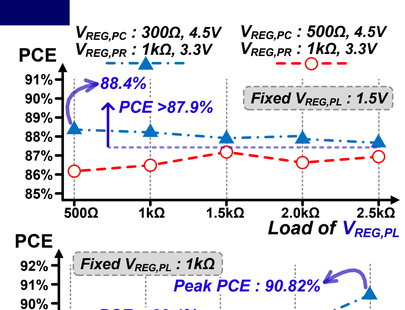


1.56mm² active area

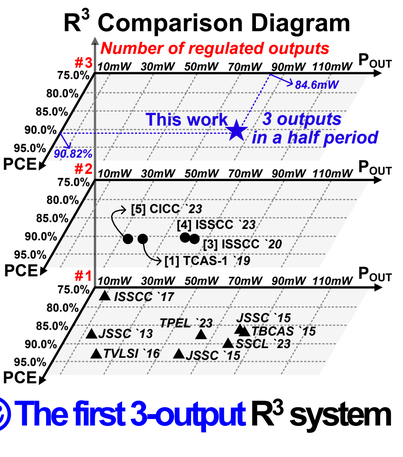
☺ 3 feedbacks in a half cycle



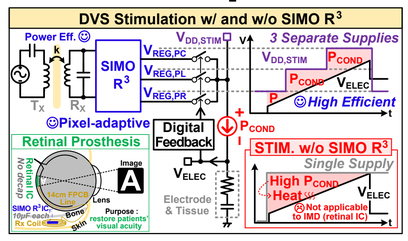
☺ 3 regulation modes

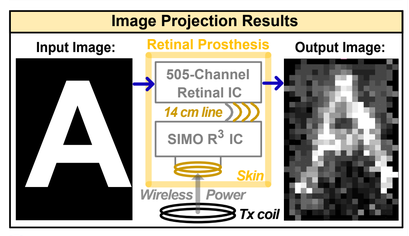


☺ Peak PCE : 90.82% @ 84.6mW



☺ The first 3-output R^3 system





☺ SIMO R^3 efficiently supplies retinal IC with DVS stimulation

Publication	CICC 2018 [4]	TCAS-I 2019 [5]	VLSI 2022 [6]	ISSCC 2020 [1]	ISSCC 2023 [2]	CICC 2023 [3]	This Work	
Overall Scheme	Dual-Output R^3						SIMO R^3	→ First trial of 3 regulation outputs
Detailed Scheme	SSDO (2X, 3X)	SSDO	Quad-mode SR-RR	PWFM	Synchronized PFM	DOVD	Peak Center, Left, Right Extraction	
Process Tech. [μm]	0.18	0.18	0.18	0.18	0.065	0.18	0.25	
Resonant Freq.	13.56 MHz	125 kHz	6.78 MHz	2 MHz & 5 MHz	40.68 MHz	13.56 MHz	2 MHz	
# Regul. Outputs	2	2	2	2	2	2	3	
# of Outputs in a Half Cycle	≤ 1	≤ 1	≤ 1	≤ 1	1	1	3	
Back Current Protection Tech.	X	X	X	X	X	X	O (for all outputs)	→ Back current protector in three outputs
# of Selectable Modes	1 (two outputs)	1 (two outputs)	1 (two outpus)	1 (two outputs)	1 (two outputs)	1 (two outputs)	3 (one or two or three outputs)	
Range of V_{OUT1}, Range of V_{OUT2}, Range of V_{OUT3}	1.4V, 2.2V – 1.8V, N/A	2.0V, 2.0V – 1.6V, N/A	5.0V, 3.7V, N/A	3.0V, 1.5V – 3.0V, N/A	2.2V, 1.1V, N/A	3.6V, 1.8V, N/A	4.5V, 3.5V – 1.0V, 3.5V – 1.0V	
$V_{OUT,MAX} - V_{OUT,MIN}$	0.4V	0.4V	N/A	1.5V	N/A	N/A	2.5V	→ Wide range
$\lvert V_{OUT1} - V_{OUT2}\rvert_{MAX}$	0.8V	0.4V	1.3V	1.5V	1.1V	1.8V	3.5V	
Peak PDL	10mW	114mW	300mW	65mW	60.5mW	81mW	135.53mW [a]	
Peak PCE @ Total load power, V_{REG1}: Vol., load V_{REG2}: Vol., load V_{REG3}: Vol,, load	79% @ total: 7.1mW, V_{REG1}: 2.75V, N/A V_{REG2}: 1.7V, N/A N/A	91.7% @ total: 42mW, V_{REG1}: 2.0V, N/A V_{REG2}: 1.8V, N/A N/A	91.8% @ total: 180mW, V_{REG1}: 5.0V, N/A V_{REG2}: 3.7V, N/A N/A	90.75% @ total: 65mW, V_{REG1}: 2.5V, 100Ω V_{REG2}: 1.5V, 2.2kΩ N/A	90.1% @ total: 60.5mW, V_{REG1}: 2.2V, 88Ω V_{REG2}: 1.1V, 220Ω N/A	91.8% @ total: 33.5mW, V_{REG1}: 3.6V, N/A V_{REG2}: 1.8V, N/A N/A	90.82% @ total: 84.6mW, V_{REG1}: 4.5V, 300Ω V_{REG2}: 3.3V, 1kΩ V_{REG3}: 2.5V, 1kΩ	→ High eff. w/ 3 outputs
Applicable to Multi-Level DVS	X	X	X	X	X	X	O	→ DVS stim.

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